

General-purpose Operational Amplifier / Comparator

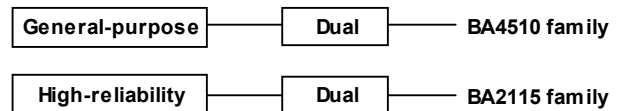


Low Saturation Operational Amplifier

BA4510F/FV, BA2115F/FVM

● Description

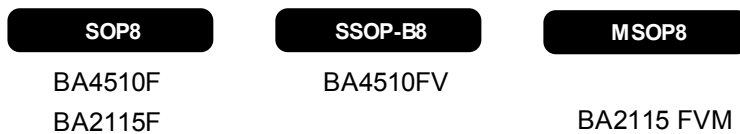
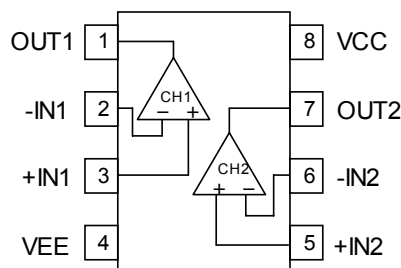
General-purpose BA4510 family and high-reliability BA2115 family integrate two independent Op-Amps and phase compensation capacitors on a single chip. These ICs are suitable for portable equipment due to low saturation output (wide output dynamic range) and are usable for audio application by low noise and distortion.



● Features

- | | |
|--|--|
| <ol style="list-style-type: none"> 1) Wide operating supply voltage
 +2.0[V] to +7.0[V] (single supply, BA4510 family)
 ±1.0[V] to ±3.5[V] (split supply, BA4510 family)
 +2.0[V] to +14.0[V] (single supply, BA2115 family)
 ±1.0[V] to ±7.0[V] (split supply, BA2115 family) 2) Wide output voltage range 3) Internal phase compensation 4) Low noise, low distortion 5) High slew rate | <ol style="list-style-type: none"> 5) Internal ESD protection
 Human body mode (HBM)±5000[V](Typ.)
 (BA2115 family) 6) Gold PAD (BA2115 family) 7) Wide temperature range
 - 20[°C] to + 75[°C](BA4510 family)
 - 40[°C] to + 85[°C](BA2115 family) |
|--|--|

● Pin Assignments



● Absolute maximum rating (Ta=25[°C])

Parameter	Symbol	Rating		Unit
		BA4510 series	BA2115 series	
Supply Voltage	VCC-VEE	10	14	V
Differential Input Voltage(*1)	Vid	VCC – VEE	14	V
Input Common-mode voltage range	Vicm	VEE to VCC	(VEE-0.3) to VEE+14	V
Operating Supply Voltage	Vopr	2 to 7(±1 to ±3.5)	2 to 14(±1 to ±7)	V
Operating Temperature	Topr	-20 to +75	-40 to +85	°C
Storage Temperature	Tstg	-55 to 125	-55 to 150	°C
Maximum junction Temperature	Tjmax	125	150	°C

Note: Absolute maximum rating item indicates the condition which must not be exceeded.

Application of voltage in excess of absolute maximum rating or use out absolute maximum rated temperature environment may cause deterioration of characteristics.

(*1) The voltage difference between inverting input and non-inverting input is the differential input voltage.
Then input terminal voltage is set to more than VEE.

● Electrical characteristics

○BA4510 family (Unless otherwise specified VCC=+2.5[V], VEE=-2.5[V], Ta=25[°C])

Parameter	Symbol	Temperature Range	Guaranteed limit			Unit	Condition
			Min.	Typ.	Max.		
Input offset voltage (*2)	Vio	25°C	-	1	6	mV	Rs=50Ω
Input offset current (*2)	Iio	25°C	-	2	200	nA	-
Input bias current	Ib	25°C	-	80	500	nA	(note)
Supply current	ICC	25°C	2.5	5.0	7.5	mA	RL=∞ All Op-Amps
Maximum output voltage	VOH	25°C	+2.0	+2.4	-	V	RL=10KΩ
	VOL	25°C	-	-2.4	-2.0	V	RL=10KΩ
Large single voltage gain	AV	25°C	60	90	-	dB	RL ≥ 10KΩ
Input common-mode voltage range	Vicm	25°C	-1.3	-	+1.5	V	-
Common-mode rejection ratio	CMRR	25°C	60	80	-	dB	-
Power supply rejection ratio	PSRR	25°C	60	80	-	dB	Rs=50Ω
Slew rate	SR	25°C	-	5.0	-	V/μs	Av=1

(*2) Absolute value

(note) Current direction: Since first input stage is composed with PNP transistor, input bias current flows out of IC.

● Electrical characteristics

○BA2115 family (Unless otherwise specified VCC=+2.5[V], VEE=-2.5[V], Ta=25[°C])

Parameter	Symbol	Temperature Range	Guaranteed limit			Unit	Condition
			Min.	Typ.	Max.		
Input offset voltage (*3)	Vio	25°C	-	1	6	mV	VOUT=0[V], Vicm=0[V]
Input offset current (*3)	Iio	25°C	-	2	200	nA	VOUT=0[V], Vicm=0[V]
Input bias current (*3)	Ib	25°C	-	150	400	nA	VOUT=0[V], Vicm=0[V]
Supply current	ICC	25°C	-	3.5	5	mA	RL=∞ All Op-Amps, VIN+=0[V]
Maximum output voltage	VOM	25°C	±2.0	±2.2	-	V	RL ≥ 2.5[kΩ]
Large single voltage gain	AV	25°C	60	80	-	dB	RL ≥ 10[kΩ], VOVT=±2[V], Vicm=0[V]
Input common-mode voltage range	Vicm	25°C	±1.5	-	-	V	-
Common-mode rejection ratio	CMRR	25°C	60	74	-	dB	Vicm=-1.5[V] to +1.5[V]
Power supply rejection ratio	PSRR	25°C	60	80	-	dB	VCC=+2[V] to +14[V]
Slew rate	SR	25°C	-	4	-	V/μs	AV=0[dB], VIN=±1[V]
Gain bandwidth product	GB	25°C	-	12	-	MHz	f=10[kHz]

(*3) Absolute value

● BA4510 family

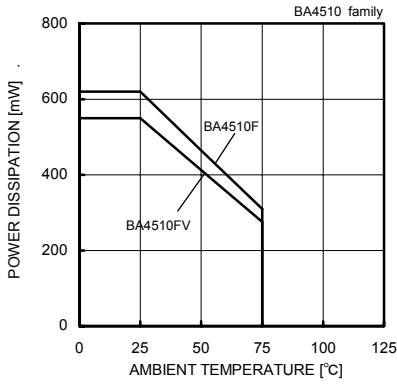


Fig.1 Derating curve

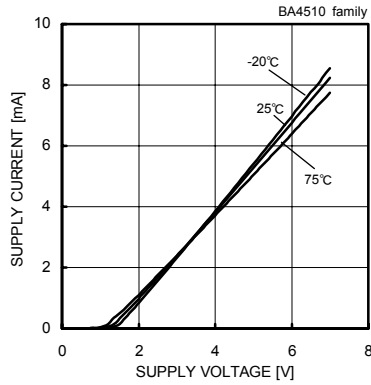


Fig.2 Supply Current – Supply Voltage

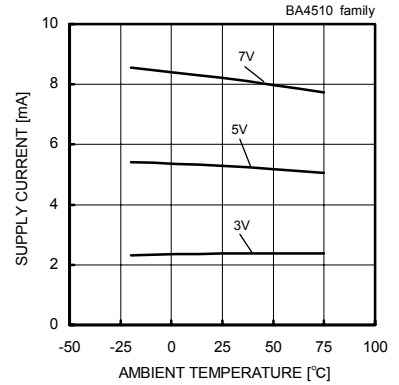


Fig.3 Supply Current – Ambient Temperature

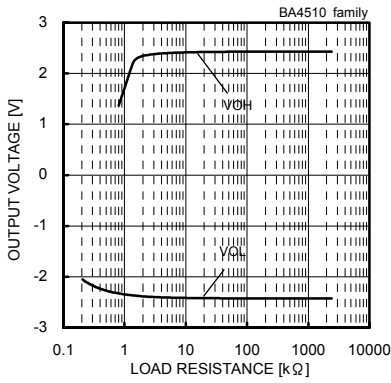


Fig.4 Output Voltage – Load Resistance
(VCC/VEE=2.5[V]/-2.5[V], Ta=25[°C])

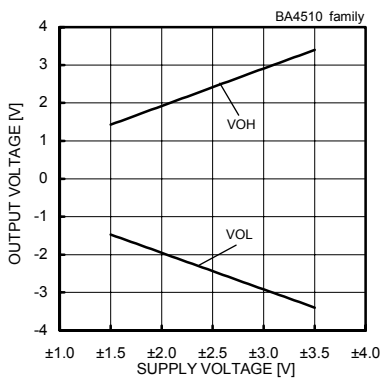


Fig.5 Output Voltage – Supply Voltage
(RL=10[kΩ], Ta=25[°C])

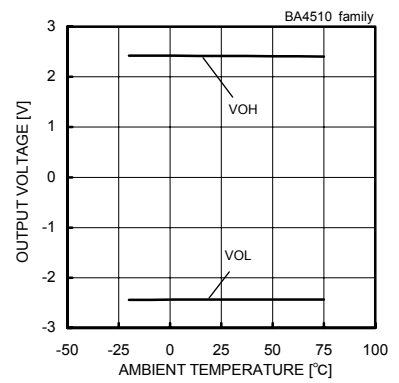


Fig.6 Output Voltage – Ambient Temperature
(VCC/VEE=2.5[V]/-2.5[V], RL=10[kΩ])

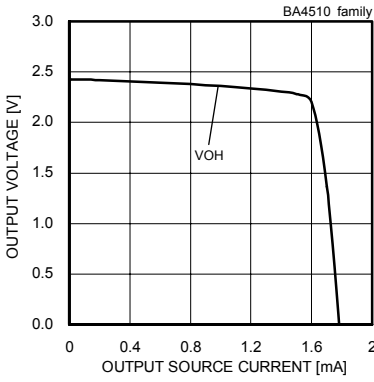


Fig.7 Output Voltage – Output Source Current
(VCC/VEE=2.5[V]/-2.5[V], Ta=25[°C])

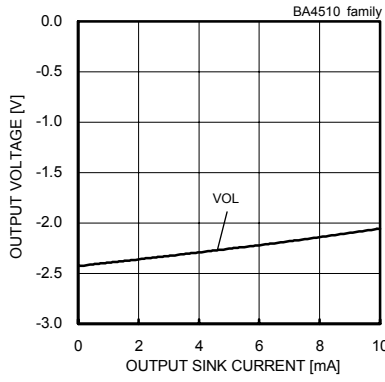


Fig.8 Output Voltage – Output Sink Current
(VCC/VEE=2.5[V]/-2.5[V], Ta=25[°C])

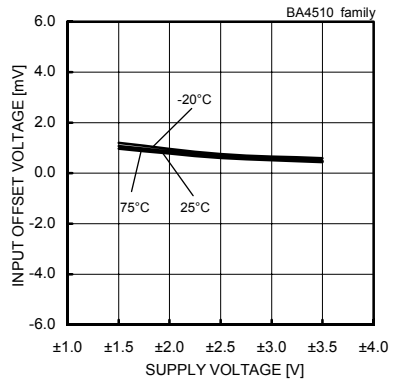


Fig.9 Input Offset Voltage – Supply Voltage
(Vcm=0[V], VOUT=0[V])

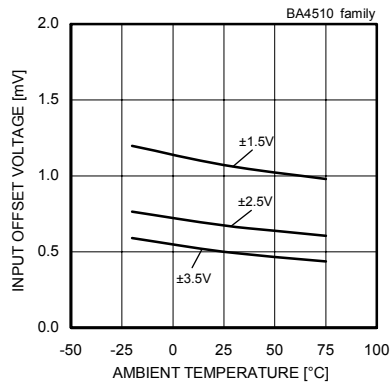


Fig.10 Input Offset Voltage – Ambient Temperature
(Vcm=0[V], VOUT=0[V])

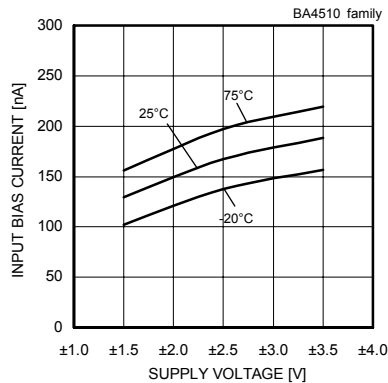


Fig.11 Input Bias Current – Supply Voltage
(Vcm=0[V], VOUT=0[V])

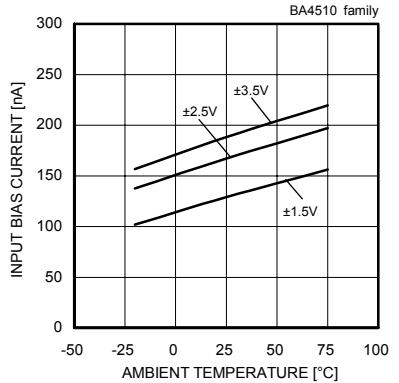


Fig.12 Input Bias Current – Ambient Temperature
(Vcm=0[V], VOUT=0[V])

(*) The date above is ability value of sample, it is not guaranteed.

● BA4510 family

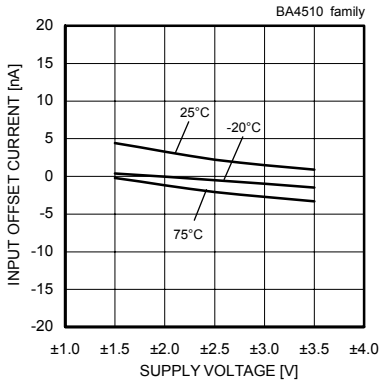


Fig. 13
Input Offset Current – Supply Voltage
($V_{icm}=0[V]$, $V_{OUT}=0[V]$)

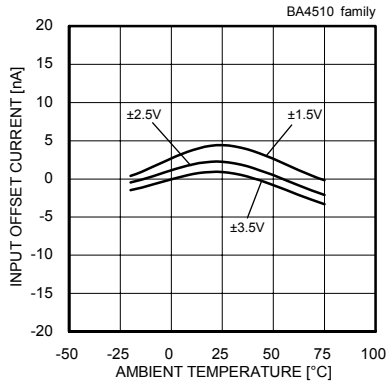


Fig. 14
Input Offset Current – Ambient Temperature
($V_{icm}=0[V]$, $V_{OUT}=0[V]$)

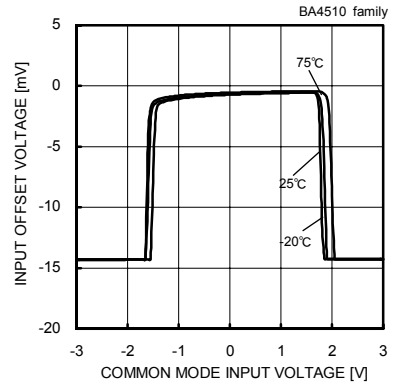


Fig. 15
Input Offset Voltage – Common Mode Input Voltage
($V_{CC}/V_{EE}=2.5[V]/-2.5[V]$)

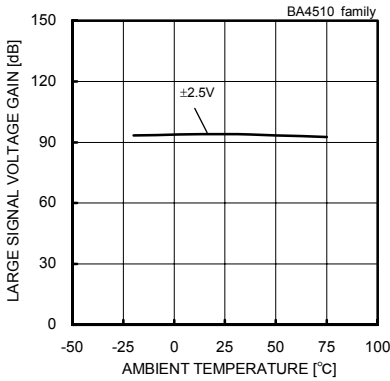


Fig. 16
Large Signal Voltage Gain – Ambient Temperature

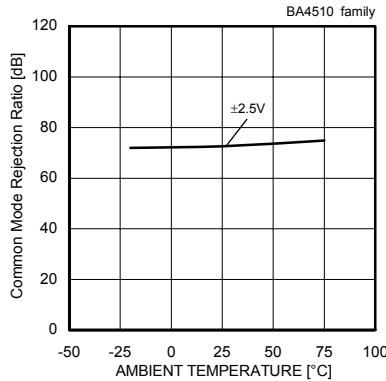


Fig. 17
Common Mode Rejection Ratio – Ambient Temperature

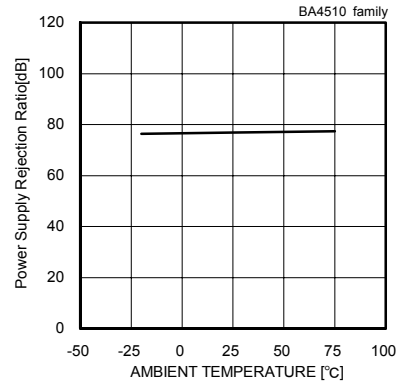


Fig. 18
Power Supply Rejection Ratio – Ambient Temperature

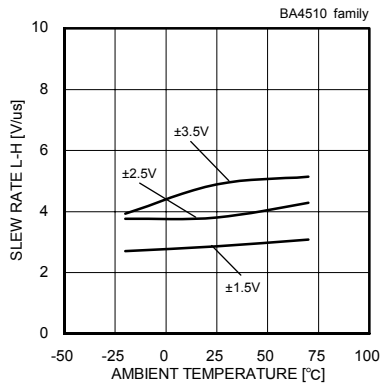


Fig. 19
Slew Rate L-H – Ambient Temperature

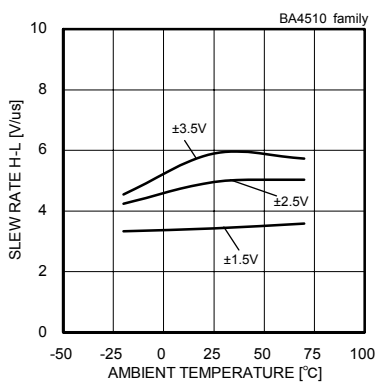


Fig. 20
Slew Rate H-L – Ambient Temperature

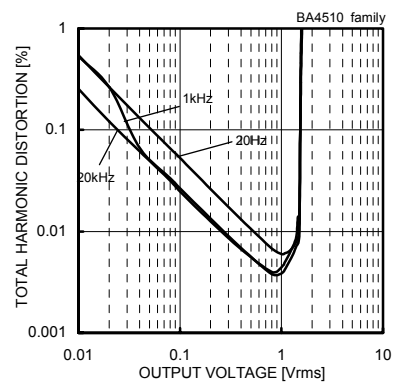


Fig. 21
Total Harmonic Distortion – Output Voltage
($V_{CC}/V_{EE}=2.5[V]/-2.5[V]$, $R_L=3[k\Omega]$, $80[kHz]$ -LPF, $T_a=25[^\circ C]$)

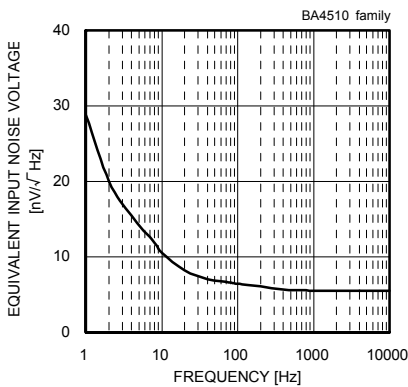


Fig. 22
Equivalent Input Noise Voltage - Frequency
($V_{CC}/V_{EE}=2.5[V]/-2.5[V]$)

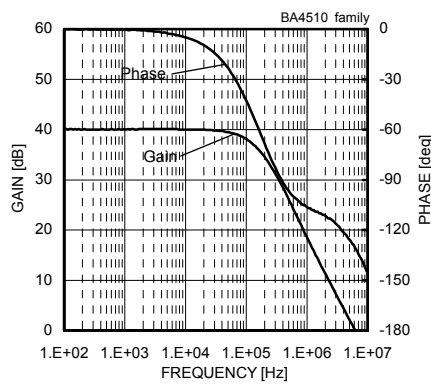


Fig. 23
Gain - Frequency
($V_{CC}/V_{EE}=2.5[V]/-2.5[V]$, $A_v=40[dB]$, $R_L=10[k\Omega]$)

(*) The date above is ability value of sample, it is not guaranteed.

● BA2115 family

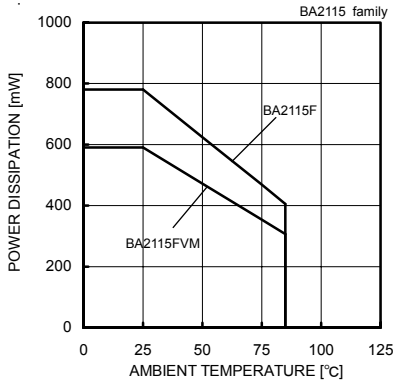


Fig.1 Derating curve

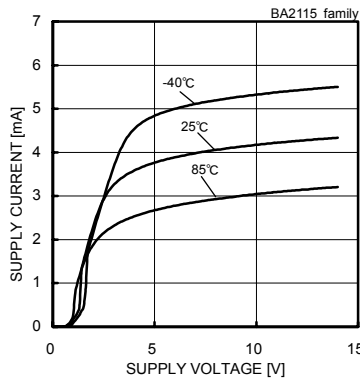


Fig.2 Supply Current - Supply Voltage

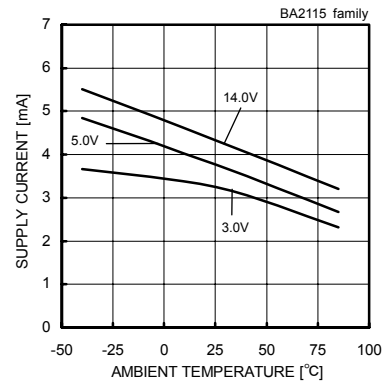


Fig.3 Supply Current - Ambient Temperature

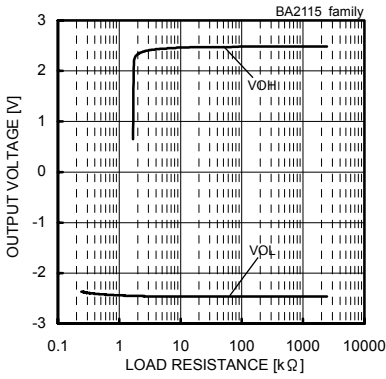


Fig.4 Output Voltage - Load Resistance (VCC/VEE=+2.5[V]/-2.5[V])

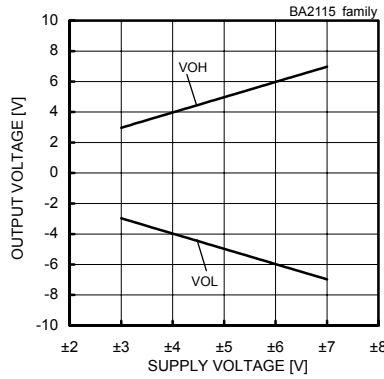


Fig.5 Output Voltage - Supply Voltage (RL=10[kΩ])

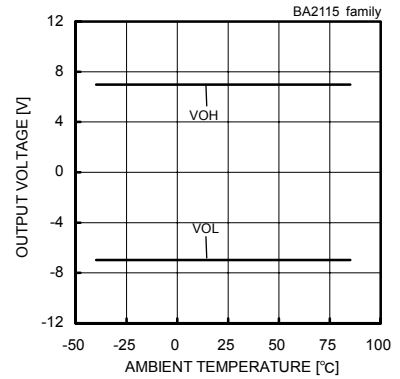


Fig.6 Output Voltage - Ambient Temperature (VCC/VEE=+7.5[V]/-7.5[V], RL=10[kΩ])

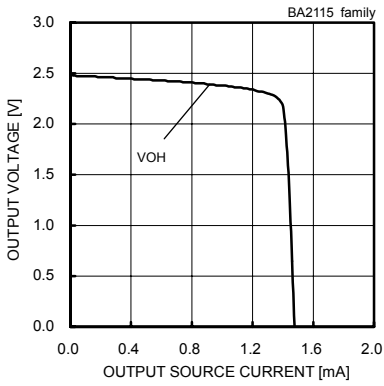


Fig.7 Output Voltage - Output Source Current (VCC/VEE=+2.5[V]/-2.5[V])

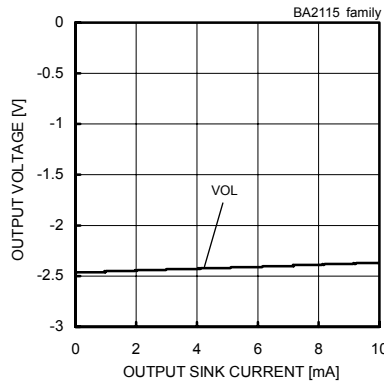


Fig.8 Output Voltage - Output Sink Current (VCC/VEE=+2.5[V]/-2.5[V])

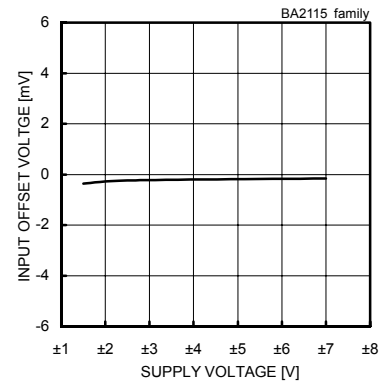


Fig.9 Input Offset Voltage - Supply Voltage (Vicm=0[V], Vout=0[V])

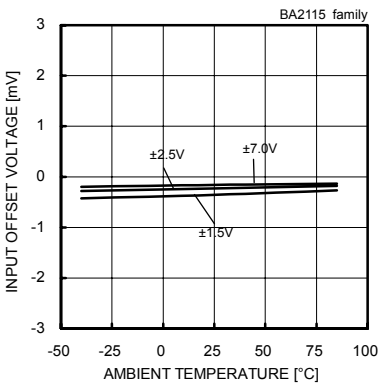


Fig.10 Input Offset Voltage - Ambient Temperature (Vicm=0[V], Vout=0[V])

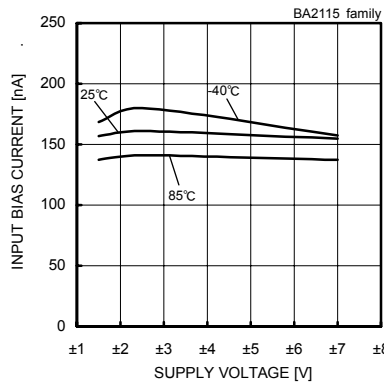


Fig.11 Input Bias Current - Supply Voltage (Vicm=0[V], Vout=0[V])

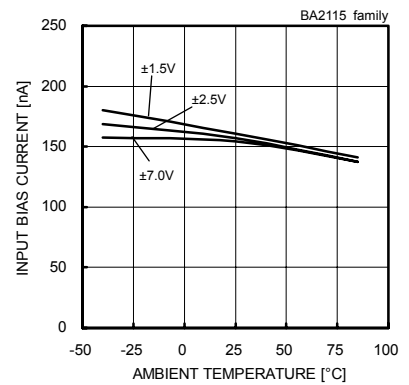


Fig.12 Input Bias Current - Ambient Temperature (Vicm=0[V], Vout=0[V])

(*) The data above is ability value of sample, it is not guaranteed.

● BA2115 family

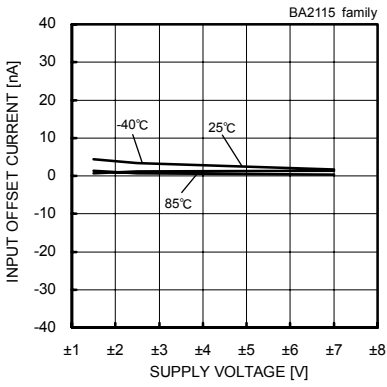


Fig. 13
Input Offset Current – Supply Voltage
($V_{icm}=0[V]$, $V_{out}=0[V]$)

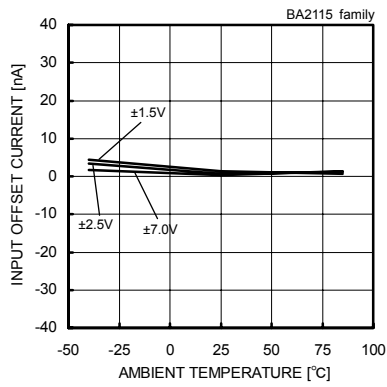


Fig. 14
Input Offset Current – Ambient Temperature
($V_{icm}=0[V]$, $V_{out}=0[V]$)

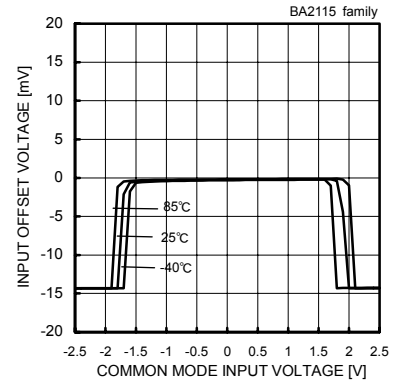


Fig. 15
Input Offset Voltage – Common Mode Input Voltage
($V_{CC}/V_{EE}=+2.5[V]/-2.5[V]$, $V_{out}=0[V]$)

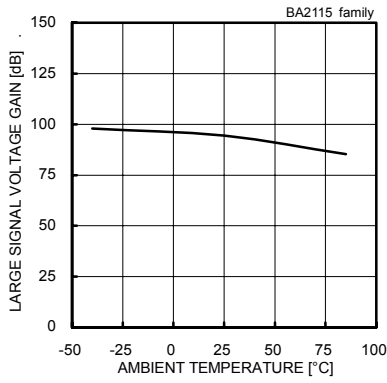


Fig. 16
Large Signal Voltage Gain – Ambient Temperature
($V_{CC}/V_{EE}=+2.5[V]/-2.5[V]$)

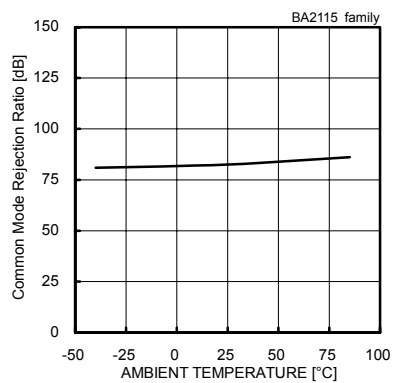


Fig. 17
Common Mode Rejection Ratio – Ambient Temperature
($V_{CC}/V_{EE}=+2.5[V]/-2.5[V]$)

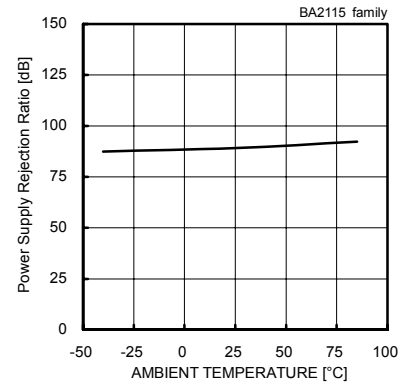


Fig. 18
Power Supply Rejection Ratio – Ambient Temperature
($V_{CC}/V_{EE}=+2.5[V]/-2.5[V]$)

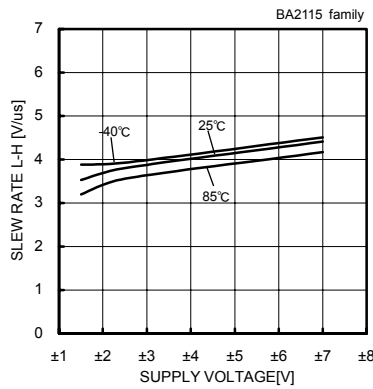


Fig. 19
Slew Rate – Supply Voltage

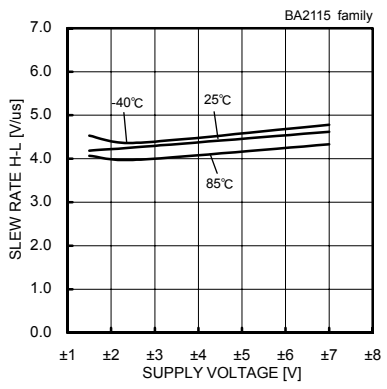


Fig. 20
Slew Rate – Supply Voltage

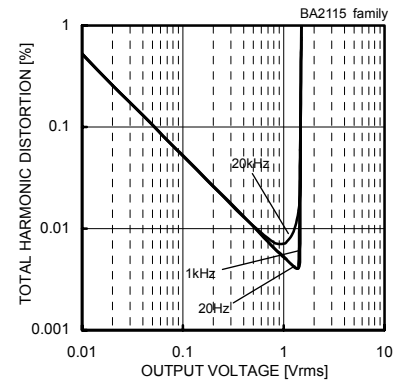


Fig. 21
Total Harmonic Distortion – Output Voltage
($V_{CC}/V_{EE}=2.5[V]/-2.5[V]$, $R_L=3[k\Omega]$, $80[kHz]$ -LPF, $T_a=25[^\circ C]$)

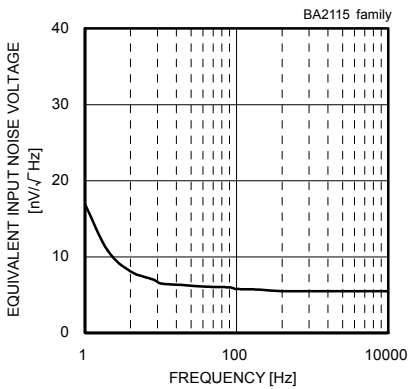


Fig. 22
Equivalent Input Noise Voltage - Frequency
($V_{CC}/V_{EE}=2.5[V]/-2.5[V]$)

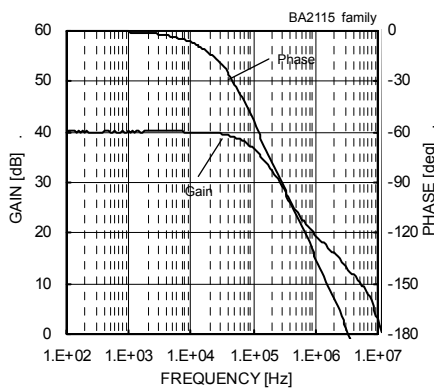


Fig. 23
Gain - Frequency
($V_{CC}/V_{EE}=2.5[V]/-2.5[V]$, $A_v=40[dB]$, $R_L=10[k\Omega]$)

(*) The date above is ability value of sample, it is not guaranteed.

● Schematic diagram

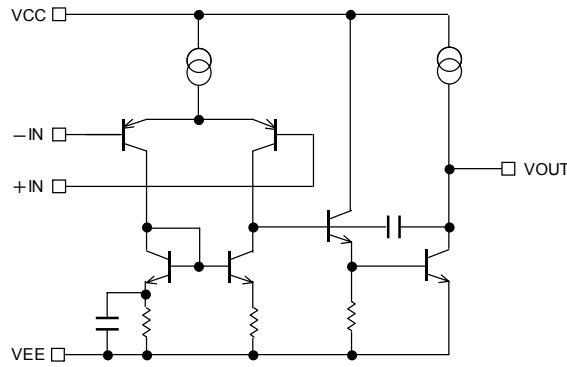


Fig.1 Simplified schematic (BA4510/BA2115)

● Test circuit1 NULL method

VCC,VEE,EK,Vicm Unit : [V]

Parameter	VF	S1	S2	S3	BA4510				BA2115				Calculation
					Vcc	VEE	EK	Vicm	Vcc	VEE	EK	Vicm	
Input offset voltage	VF1	ON	ON	OFF	+2.5	-2.5	0	0	+2.5	-2.5	0	0	1
Input offset current	VF2	OFF	OFF	OFF	+2.5	-2.5	0	0	+2.5	-2.5	0	0	2
Input bias current	VF3	OFF	ON	OFF	+2.5	-2.5	0	0	+2.5	-2.5	0	0	3
	VF4	ON	OFF	OFF	+2.5	-2.5	0	0	+2.5	-2.5	0	0	
Large signal voltage gain	VF5	ON	ON	ON	+2.5	-2.5	-1.0	0	+2.5	-2.5	-1.0	0	4
	VF6	ON	ON	ON	+2.5	-2.5	+1.0	0	+2.5	-2.5	+1.0	0	
Common-mode rejection ratio (Input common-mode voltage range)	VF7	ON	ON	OFF	+1.5	-3.5	-1.0	0	+1.5	-3.5	-1.0	0	5
	VF8	ON	ON	OFF	+3.5	-1.5	+1.0	0	+3.5	-1.5	+1.0	0	
Power supply rejection ratio	VF9	ON	ON	OFF	+1.25	-1.25	0	0	+0.75	-1.25	0	0	6
	VF10	ON	ON	OFF	+3.0	-3.0	0	0	+7.0	-7.0	0	0	

— Calculation —

1. Input offset Voltage (Vio)

$$V_{io} = \frac{|VF1|}{1 + R_f / R_s} \text{ [V]}$$

2. Input offset current (Iio)

$$I_{io} = \frac{|VF2 - VF1|}{R_i \times (1 + R_f / R_s)} \text{ [A]}$$

3. Input bias current (Ib)

$$I_b = \frac{|VF4 - VF3|}{2 \times R_i \times (1 + R_f / R_s)} \text{ [A]}$$

4. Large signal voltage gain (Av)

$$A_v = 20 \times \text{Log} \frac{\Delta E_K \times (1 + R_f / R_s)}{|VF5 - VF6|} \text{ [dB]}$$

5. Common-mode rejection ratio (CMRR)

$$\text{CMRR} = 20 \times \text{Log} \frac{\Delta V_{icm} \times (1 + R_f / R_s)}{|VF8 - VF7|} \text{ [dB]}$$

6. Power supply rejection ratio (PSRR)

$$\text{PSRR} = 20 \times \text{Log} \frac{\Delta V_{cc} \times (1 + R_f / R_s)}{VF10 - VF9} \text{ [dB]}$$

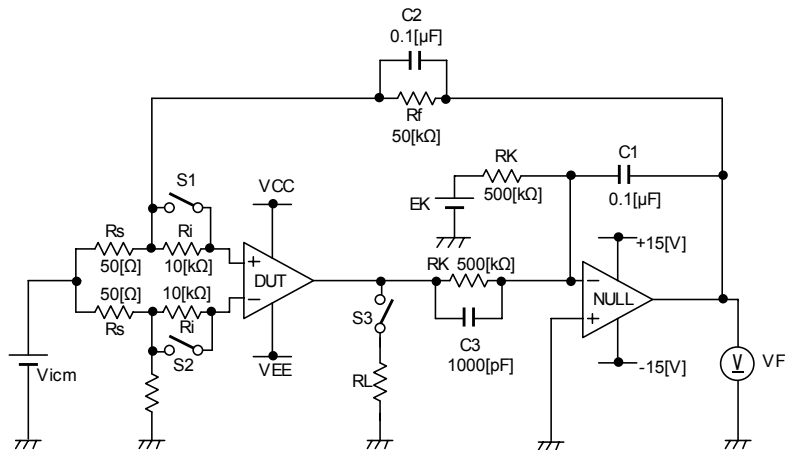


Fig2. Test circuit 1 (one channel only)

● Test circuit2 switch condition

SW No.	SW 1	SW 2	SW 3	SW 4	SW 5	SW 6	SW 7	SW 8	SW 9	SW 10	SW 11	SW 12	SW 13	SW 14
Supply current	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
最大出力電圧	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
Slew rate	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
利得帯域幅	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
全高調波歪率	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF
Input noise voltage (*1)	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF

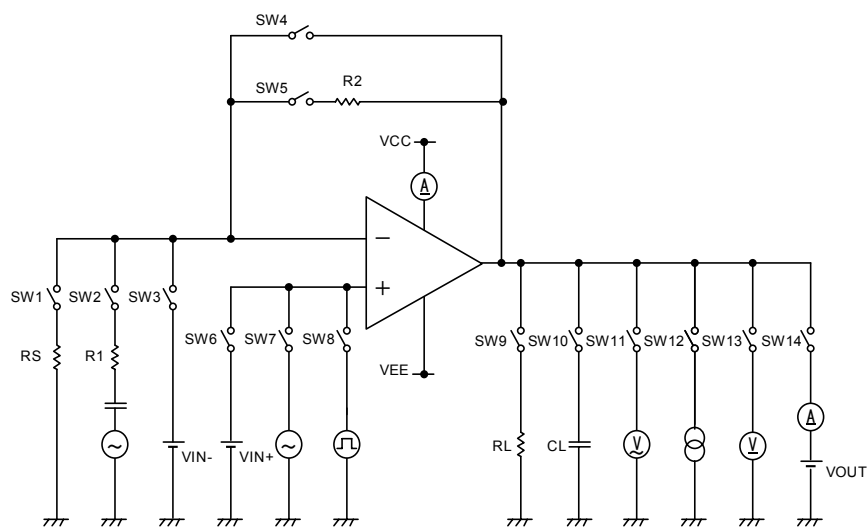


Fig3. Test circuit2 (one channel only)

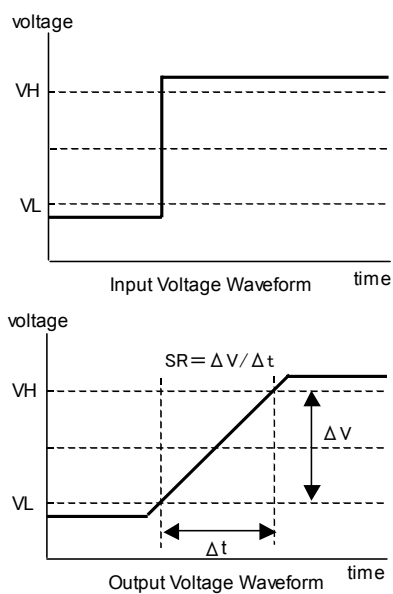


Fig4. Slew rate input output wave

● Description of electrical characteristics

Described here are the terms of electric characteristics used in this technical note. Items and symbols used are also shown.

Note that item name and symbol and their meaning may differ from those on another manufacture's document or general document.

1. Absolute maximum ratings

Absolute maximum rating item indicates the condition which must not be exceeded. Application of voltage in excess of absolute Maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

- 1.1 Power supply voltage (VCC—VEE)
Indicates the maximum voltage that can be applied between the positive power supply terminal and negative power supply terminal Without deterioration or destruction of characteristics of internal circuit.
- 1.2 Differential input voltage (Vid)
Indicates the maximum voltage that can be applied between non-inverting terminal and inverting terminal without deterioration and Destruction of characteristics of IC.
- 1.3 Input common-mode voltage range (Vicm)
Indicates the maximum voltage that can be applied to non-inverting terminal and inverting terminal without deterioration or destruction of Characteristics. Input common-mode voltage range of the maximum ratings not assure normal operation of IC. When normal Operation of IC is desired, the input common-mode voltage of characteristics item must be followed.
- 1.4 Power dissipation (Pd)
Indicates the power that can be consumed by specified mounted board at the ambient temperature 25°C(normal temperature). As for Package product, Pd is determined by the temperature that can be permitted by IC chip in the package (maximum junction temperature) and thermal resistance of the package

2. Electrical characteristics item

- 2.1 Input offset voltage (Vio)
Indicates the voltage difference between non-inverting terminal and inverting terminal. It can be translated into the input voltage difference required for setting the output voltage at 0 [V]
- 2.2 Input offset current (Iio)
Indicates the difference of input bias current between non-inverting terminal and inverting terminal.
- 2.3 Input bias current (Ib)
Indicates the current that flows into or out of the input terminal. It is defined by the average of input bias current at non-inverting terminal and input bias current at inverting terminal.
- 2.4 Circuit current (ICC)
Indicates the IC current that flows under specified conditions and no-load steady status.
- 2.5 Maximum output voltage (VOM)
Indicates the range of voltage that can be output by IC under specified load condition. It is general divided into high Level output voltage and low level output voltage.
- 2.6 Large signal voltage gain (AV)
Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting terminal and inverting terminal. It is normally the amplifying rate (gain) with reference to DC voltage.
$$A_v = (\text{Output voltage fluctuation}) / (\text{Input offset fluctuation})$$
- 2.7 Input common-mode voltage range (Vicm)
Indicates the input voltage range where IC operates normally.
- 2.8 Common-mode rejection ratio (CMRR)
Indicates the ratio of fluctuation of input offset voltage when in-phase input voltage is changed. It is normally the fluctuation of DC.
$$\text{CMRR} = (\text{Change of Input common-mode voltage}) / (\text{Input offset fluctuation})$$
- 2.9 Power supply rejection ratio (PSRR)
Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed. It is normally the fluctuation of DC.
$$\text{PSRR} = (\text{Change of power supply voltage}) / (\text{Input offset fluctuation})$$
- 2.10 Channel separation (CS)
Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.
- 2.11 Slew rate (SR)
Indicates the time fluctuation ratio of voltage output when step input signal is applied
- 2.12 Unity gain frequency (ft)
Indicates a frequency where the voltage gain of Op-Amp is 1.
- 2.13 Total harmonic distortion + Noise (THD+N)
Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel
- 2.14 Input referred noise voltage (Vn)
Indicates a noise voltage generated inside the operational amplifier equivalent by ideal voltage source connected in series with input terminal

● Derating curve

Power dissipation (total loss) indicates the power that can be consumed by IC at Ta=25°C (normal temperature). IC is heated when it consumed power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called thermal resistance, represented by the symbol θ_{j-a} [°C/W]. The temperature of IC inside the package can be estimated by this thermal resistance. Fig.6 (a) shows the model of thermal resistance of the package. Thermal resistance θ_{ja} , ambient temperature Ta, junction temperature Tj, and power dissipation Pd can be calculated by the equation below :

$$\theta_{ja} = (T_j - T_a) / P_d \quad [^{\circ}\text{C}/\text{W}] \quad \dots \dots (1)$$

Derating curve in Fig.6 (b) indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θ_{ja} . Thermal Resistance θ_{ja} depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Fig 2(a), (b) show a derating curve for an example of BA4510family, BA2115family.

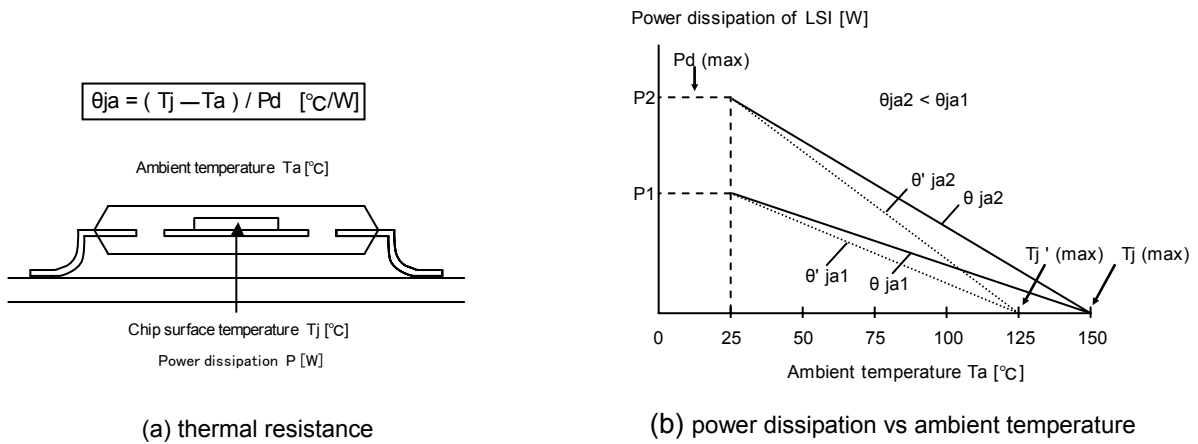
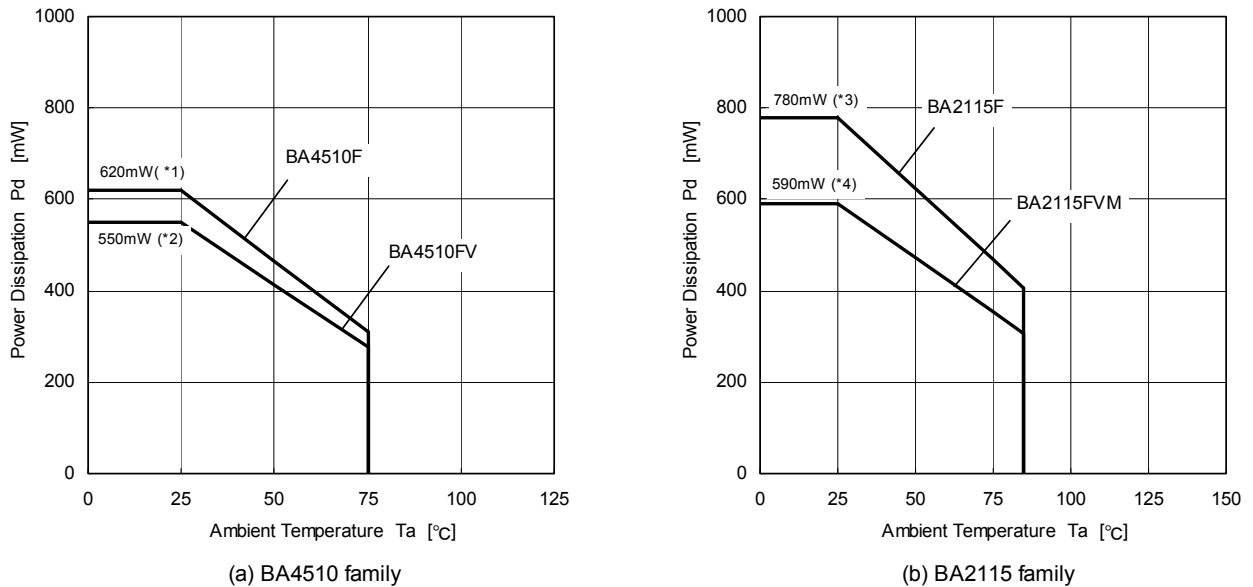


Fig.1 thermal resistance and power dissipation



(*1)	(*2)	(*3)	(*4)	単位
6.2	5.5	6.2	4.7	[mW/°C]

When using the unit above Ta=25[°C], subtract the value above per degree[°C]. Permissible dissipation is the value when FR4 glass epoxy board 70[mm]×70[mm]×1.6[mm] (cooper foil area below 3[%]) is mounted.

Fig2. Derating curve

● Cautions on use

1) Processing of unused circuit

It is recommended to apply connection (see the Fig.1) and set the noninverting input terminal at the potential within input common-mode voltage range (V_{icm}), for any unused circuit.1)

2) Input voltage

Applying $V_{EE}+14[V]$ (BA2115 family) to the input terminal is possible without causing deterioration of the electrical characteristics or destruction, irrespective of the supply voltage. However, this does not ensure normal circuit operation.

Please note that the circuit operates normally only when the input voltage is within the common mode input voltage range of the electric characteristics.

3) Maximum output voltage

Because the output voltage range becomes narrow as the output current increases, design the application with margin by considering changes in electrical characteristics and temperature characteristics.

4) Short-circuit of output terminal

When output terminal and VCC or VEE terminal are shorted, excessive output current may flow under some conditions, and heating may destroy IC. It is necessary to connect a resistor as shown in Fig.10, thereby protecting against load shorting.

5) Power supply (split supply / single supply) in used

Op amp operates when specified voltage is applied between VCC and VEE. Therefore, the single supply Op Amp can be used for split supply Op Amp as well.

6) Power dissipation (Pd)

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

6) Short-circuit between pins and wrong mounting

Pay attention to the assembly direction of the ICs. Wrong mounting direction or shorts between terminals, GND, or other components on the circuits, can damage the IC.

7) Use in strong electromagnetic field

Using the ICs in strong electromagnetic field can cause operation malfunction.

8) Radiation

This IC is not designed to be radiation-resistant.

9) Handling of IC

When stress is applied to IC because of deflection or bend of board, the characteristics may fluctuate due to piezoelectric (piezo) effect.

10) Inspection on set board

During testing, turn on or off the power before mounting or dismantling the board from the test Jig.

Do not power up the board without waiting for the output capacitors to discharge. The capacitors in the low output impedance terminal can stress the device. Pay attention to the electro static voltages during IC handling, transportation, and storage.

11) Output capacitor

When VCC terminal is shorted to VEE (GND) potential and an electric charge has accumulated on the external capacitor, connected to output terminal, accumulated charge may be discharged VCC terminal via the parasitic element within the circuit or terminal protection element. The element in the circuit may be damaged (thermal destruction). When using this IC for an application circuit where there is oscillation, output capacitor load does not occur, as when using this IC as a voltage comparator. Set the capacitor connected to output terminal below $0.1[\mu F]$ in order to prevent damage to IC.

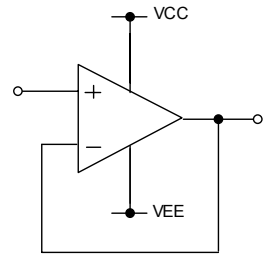


Fig.1 The example of application circuit for unused op-amp

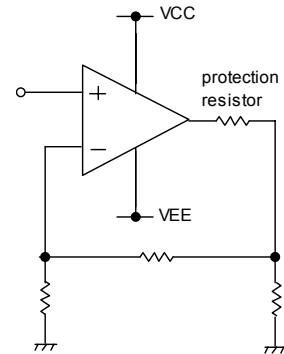
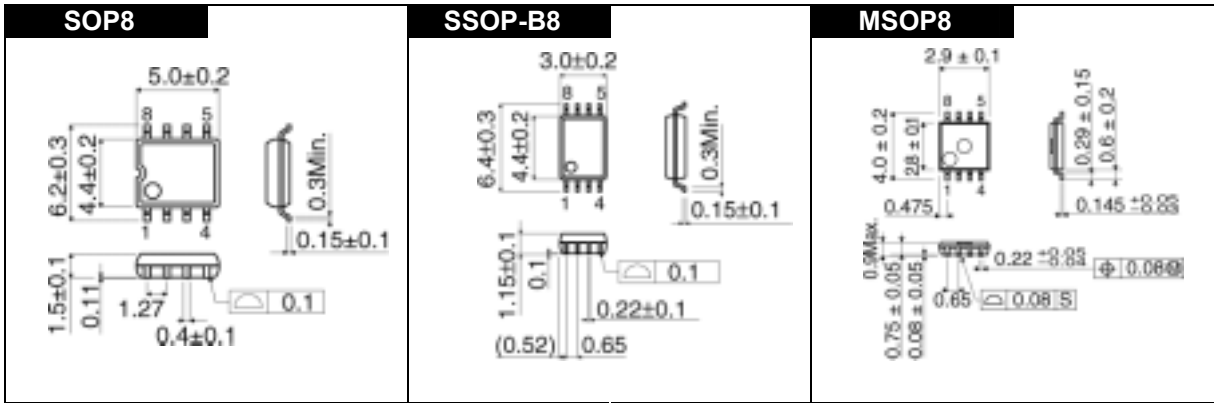


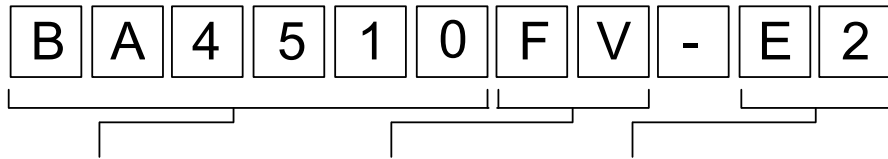
Fig.2 The example of output short protection

● Dimensions



● Model number construction

- Specify the product by the model number when placing an order.
- Make sure of the combinations of items.
- Start with the leftmost space without leaving any empty space between characters.



ROHM product name

- BA4510
- BA2115

Package type

- F : SOP8
- FV : SSOP-B8
- FVM : MSOP8

E2 Embossed tape on reel with pin 1 near far when pulled out
 TR Embossed tape on reel with pin 1 near far when pulled out

Packing specification reference

Package	Packing specification name	Quantity	Embossed carrier tape
SOP8/ SSOP-B8	E2	2500	
MSOP8	TR	3000	

Notes

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